## REMARKS

In response to the Office Action mailed on November 28, 2006, Applicant respectfully requests reconsideration. Claims 1-12 were previously pending in this application. By this amendment, claims 1, 3, 6, 7, 9 and 11 are amended. As a result, claims 1-12 are pending for examination with claims 1, 3, 6, 7, 9 and 11 being independent. No new matter has been added.

### I. Allowable Subject Matter

Applicant appreciates the Examiner's indication of allowable subject matter in claims 3, 4, 7, 8, 11 and 12. In particular, the Examiner indicates that claims 3, 4, 7, 8, 11 and 12 would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims and rewritten to overcome the rejection under 35 U.S.C. §101. Applicant respectfully points out that claim 3 (from which claim 4 depends), claim 7 (from which claim 8 depends) and claim 11 (from which claim 12 depends) were rewritten in independent form in the previous Response incorporating all the subject matter of their base and intervening claims. Claims 3, 7 and 11 are amended herein to overcome the rejection under 35 U.S.C. §101, as discussed in Section II below. Therefore, claims 3, 4, 7, 8, 11 and 12 are believed to be in allowable condition.

### II. Rejections Under 35 U.S.C. § 101

The Office Action rejects claims 1-12 under 35 U.S.C. §101 because the claims purportedly do not "produce a useful, concrete and tangible result," as required by the holding in *State Street Bank & Trust Co. v. Signature Financial Group, Inc.* While Applicant disagrees with the Office Action as to what the *State Street* holding requires, claims 1, 3, 6, 7, 9 and 11 have been amended such that the claims produce a useful, concrete and tangible result even under the interpretation of the standard alleged by the Office Action.

In particular, claim 1 has been amended to recite "providing the loop top instruction address to an instruction fetch stage of the pipelined processor if it is determined that the next instruction is the loop bottom instruction, and fetching the loop top instruction prior to completing a decoding of the loop bottom instruction," which produces a useful, concrete and tangible result even under the standard alleged by the Office Action.

Claim 3 has been amended to recite "changing a state of a loop bottom register if it is determined that the next instruction is the loop bottom instruction to indicate to the pipelined processor that a loop top instruction should be fetched," which would produce a useful, concrete and tangible result as indicated by the Office Action in the Response to Arguments section.

Claim 6 has been amended to recite that the loop bottom detector is "configured to provide the loop top instruction to the instruction fetch stage prior to completing a decoding of the loop bottom instruction if the loop bottom detector determines the next instruction is the loop bottom instruction," which produces a useful, concrete and tangible result even under the standard alleged by the Office Action.

Claim 7 has been amended to recite that "the loop bottom detector is configured to change the state of the loop bottom register if it is determined that the next instruction is the loop bottom instruction," which would produce a useful, concrete and tangible result as indicated by the Office Action in the Response to Arguments section.

Claim 9 has been amended to recite means "configured to provide the loop top instruction to the means for fetching instructions prior to completing a decoding of the loop bottom instruction if the next instruction is determine to be the loop bottom instruction," which produces a useful, concrete and tangible result even under the standard alleged by the Office Action.

Claim 11 has been amended to recite "means for changing a state of a loop bottom register when it is determined that the next instruction is the loop bottom instruction," which would produce a useful, concrete and tangible result as indicated by the Office Action in the Response to Arguments section.

Accordingly, each of the independent claims has been amended such that the claims would produce a useful, concrete and tangible result even under the standard asserted in the Office Action. Therefore, Applicant respectfully requests that the rejection under 35 U.S.C. §101 be withdrawn.

## II. Rejections Under 35 U.S.C. § 103

The Office Action rejects claims 1, 2, 5, 6, 9 and 10 as being unpatentable over U.S. Publication No. 2002/0078333) in view of Applicant's background. While Applicant disagrees with this rejection, Applicant has amended the claims to clearly distinguish over the alleged combination.

Initially, Applicant respectfully points out that the Office Action has improperly used Applicant's own disclosure as evidence that it would have been obvious to modify Inoue. Some aspects of the invention derive from the recognition that variable length instructions can not be treated in the same manner as uniform length instructions. In particular, early detection of loop bottom instructions is complicated by the fact that variable length instructions conventionally prevent loop bottom instructions from being detected prior to decoding the instruction. This recognition is Applicant's insight and cannot be used as motivation to modify Inoue. However, because Applicant has amended the claims to distinguish over the alleged combination, the alleged combination will not be argued in further detail herein. However, Applicant reserves the right to argue this combination in the future if deemed necessary.

A. Inoue

Inoue is directed to using multiple pipelines in parallel to improve the efficiency of hardware loops (Abstract). In particular, Inoue discusses methods for efficiently setting up hardware loops and efficiently using resources to implement the established hardware loops. Inoue describes one problem with conventional hardware loop setup. Conventional hardware loops may be initialized by the loop setup instruction by writing the boundaries of the hardware loop to architectural registers (paragraph [0019]). After the hardware loop is initialized, the hardware loop may operate in the pipeline until the exit conditions have been satisfied (paragraph [0019]). Inoue reports that because architectural registers are written only when the loop setup instruction exits the write-back stage, the architectural registers may not be updated until several clock cycles after the loop instruction enters the pipeline resulting in delays in setting up hardware loops (paragraph [0020]).

To address issues related to loop set up penalties, Inoue describes implementing a set of early registers to store hardware loop boundaries. Because the early registers can be written before the loop setup instruction is committed, implementing early registers may reduce the time it takes to setup hardware loops (paragraph [0022]). However, Inoue is directed to decreasing delays in setting up the hardware loops, not in delays associated with detecting loop bottom instructions. Indeed, Inoue only mentions the loop bottom instruction in the context of setting up the hardware loop. Paragraph [0030] of Inoue states:

> The top and bottom values may indicate which instruction is the top of the loop, and which instruction is the bottom of the loop. The top and bottom values in the loop setup instruction, however, may be program counter (PC) relative. Therefore, a calculation (40) in AC stage may be used to obtain the top and bottom values that will be written to ETop 34A and EBot 34B registers respectively. After the loop setup instruction enters EX 1 (41), the top and bottom values may be written to the ETop 34A and EBot 34B registers (42).

Inoue is completely silent with respect to detecting the loop bottom instruction during execution of the hardware loop. It is true that Inoue naturally detects the loop bottom instruction in some manner. However, Inoue does not provide any details in this respect. In particular, Inoue nowhere mentions how or when the loop bottom instruction is detected and what effect it has on executing the loop, for example, preventing stalls that are incurred in conventional loop bottom detection due to the inability to make this determination until the loop bottom instruction has been fully decoded. Inoue is completely silent with respect to detecting the loop bottom instruction and, upon detection, fetching the loop top instruction prior to decoding the loop bottom instruction.

Claim 1, as amended, recites a method for processing variable width instructions in a pipelined processor, comprising decoding instructions to identify a loop setup instruction having a loop setup instruction address to determine a loop top offset indicative of a loop top instruction address of a loop top instruction and a loop bottom offset indicative of a loop bottom instruction address of a loop bottom instruction, decoding a current instruction following the loop setup instruction, the current instruction having ~~an~~ a current instruction address and a current instruction width, determining if a next instruction to be decoded is the loop bottom instruction based, at least in part, on the current instruction address, the current instruction width, the loop setup instruction address and the loop bottom offset, providing the loop top instruction address to an instruction fetch stage of the pipelined processor if it is determined that the next instruction is the loop bottom instruction, and fetching the loop top instruction prior to completing a decoding of the loop bottom instruction.

Nowhere does Inoue disclose or suggest determining if a next instruction to be decoded is the loop bottom instruction and "providing the loop top instruction address to an instruction fetch stage of the pipelined processor if it is determined that the next instruction is the loop bottom instruction, and fetching the loop top instruction prior to completing a decoding of the loop bottom

instruction," as recited in claim 1. Applicant's background does not provide any disclosure to cure the deficiency of Inoue in this respect. Therefore, claim 1 patentably distinguishes over the combination of Inoue and Applicant's background and is in allowable condition.

Claims 2 and 5 depend from claim 1 and are allowable based at least upon their dependency.

Claim 6, as amended, recites an apparatus for processing variable width instructions in a pipeline processor, comprising an instruction decoder configured to decode a loop setup instruction, having a loop setup instruction address, to obtain a loop top offset indicative of a loop top instruction address of a loop top instruction and a loop bottom offset indicative of a loop bottom instruction address of a loop bottom instruction and configured to decode instructions following the loop setup instruction, each having an instruction address, to obtain an instruction width, an instruction fetch stage configured to fetch instructions to be decoded by the instruction decoder, registers for holding the loop setup instruction address and the loop bottom offset, respectively, and a loop bottom detector-configured to determine if a next instruction to be decoded is the loop bottom instruction based, at least in part, on a current instruction address and current instruction width of a current instruction being decoded by the instruction decoder, and configured to provide the loop top instruction to the instruction fetch stage prior to completing a decoding of the loop bottom instruction if the loop bottom detector determines the next instruction is the loop bottom instruction.

Nowhere does Inoue disclose or suggest a loop bottom detector configured to determine if a next instruction to be decoded is the loop bottom instruction and "configured to provide the loop top instruction to the instruction fetch stage prior to completing a decoding of the loop bottom instruction if the loop bottom detector determines the next instruction is the loop bottom instruction," as recited in claim 6. Applicant's background does not provide any disclosure to cure the deficiency of Inoue in this respect. Therefore, claim 6 patentably distinguishes over the combination of Inoue and Applicant's background and is in allowable condition.

Claim 9, as amended, recites an apparatus for processing variable width instructions in a pipelined processor, comprising means for decoding a loop setup instruction, having a loop setup instruction address, to obtain a loop top offset indicative of a loop top instruction address of a loop top instruction and a loop bottom offset indicative of a loop bottom instruction address of a loop bottom instruction and for decoding instructions following the loop setup instruction, each having

an instruction address, to obtain an instruction width, means for fetching instructions to be decoded by the means for decoding, means for holding the loop setup instruction address and the loop bottom offset, and means for determining if a next instruction to be decoded is the loop bottom instruction based, at least in part, on a current instruction address and current instruction width of a current instruction being decoded by the instruction decoder, and configured to provide the loop top instruction to the means for fetching instructions prior to completing a decoding of the loop bottom instruction if the next instruction is determine to be the loop bottom instruction.

Nowhere does Inoue disclose or suggest means for determining if a next instruction to be decoded is the loop bottom instruction and "configured to provide the loop top instruction to the means for fetching instructions prior to completing a decoding of the loop bottom instruction if the next instruction is determine to be the loop bottom instruction," as recited in claim 9. Applicant's background does not provide any disclosure to cure the deficiency of Inoue in this respect. Therefore, claim 9 patentably distinguishes over the combination of Inoue and Applicant's background and is in allowable condition.

Claim 10 depends from claim 9 and is allowable for at least the same reasons.

## CONCLUSION

In view of the above remarks, Applicant believes the pending application is in condition for allowance, and a Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
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